Exhibit 11

UNITED STATES DISTRICT COURT
DISTRICT OF MASSACHUSETTS

ACQIS, LLC, **Plaintiff,** **v.** **EMC CORPORATION,** **Defendant.**	**C.A. No. 1:14-cv-13560-ADB** **PUBLIC VERSION**

PLAINTIFF ACQIS LLC'S REBUTTAL TO EMC'S STATEMENT OF MATERIAL FACTS IN SUPPORT OF DEFENDANT EMC CORPORATION'S MOTION FOR SUMMARY JUDGMENT OF NON-INFRINGEMENT (D.I. 504)

Pursuant to Local Rule 56.1, Plaintiff ACQIS LLC submits this Rebuttal to EMC's Statement of Material Facts in Support of Its Opposition to EMC's Motion for Summary Judgment of Non-Infringement (D.I. 504, ("EMC's SMF"), showing that genuine issues of material fact remain to be tried.

1. With respect to EMC's SMF ¶3, although ACQIS does not presently assert infringement under the doctrine of equivalents, should the Court alter its claim constructions, ACQIS may use evidence in the record to establish infringement of the asserted claims, including under the doctrine of equivalents. For example, Mr. Gafford testified that commands defined in the PCI Local Bus Specification and commands in PCI Express perform the same function, in the same way, to achieve the same result. (Gafford Dep. (5/18/2018), Ex. 1 at 664:10-665:18; Gafford Report, Appx. 27 at ¶¶238-242.)

2. ACQIS disputes EMC's SMF ¶8. The PCI Local Bus Specification defines a "transaction" as "an address phase plus one or more data phases." (PCI Local Bus Specification ("PCI LBS"), Appx. 65 at -948.)[1] The PCI Local Bus Specification defines a "phase" as "[o]ne or more clocks in which a single unit of information is transferred." (PCI LBS, Appx. 65 at -947 (emphasis added).) An *address phase* is "a single address transfer in one clock for a single address cycle and two clocks for a dual address cycle," and a *data phase* is "one transfer state plus zero or more wait states." (PCI LBS, Appx. 65 at -947.) A "transfer state" is defined as "[a]ny bus clock, during a data phase, in which data is transferred." (PCI LBS, Appx. 65 at -948 (emphasis added).) A Person of ordinary skill ("POSA") would understand that a transaction, according the PCI Local Bus Specification, defines a transaction as the information

[1] All "Appx." documents cited herein are attached to the Declaration of James Brogan in Support of ACQIS's Statement of Material Facts in Support of Its Motions for Summary Judgment. (D.I. 529-1.)

communicated in the address phase and data phase. (Declaration of Thomas A. Gafford Regarding EMC's Motion for Summary Judgment of Non-Infringement ("Gafford Decl.") at ¶19.)

3. ACQIS disputes EMC's SMF ¶9. The claims of the asserted patents describe communicating transactions according to the PCI Local Bus Specification in serial form. (*See, e.g.*, '873 patent, Appx. 9 at cl. 9, 61; '468 patent, Appx. 14 at cl. 29; Lindenstruth IPR Decl., D.I. 189-4 at ¶119 ("I note that a PCI bus is parallel and the claims discuss communicating PCI bus transactions serially, so the claims do not require that the PCI bus transaction occur on a PCI bus; they require the address and data phases of a PCI bus transaction, which include the PCI address and bus command information during the address phase, and the PCI data and byte enables during the data phases.") (citations omitted); 189-5 at ¶114 (same); Gafford Decl. at ¶¶13-19.)

4. ACQIS disputes EMC's SMF ¶12. The PCI Local Bus Specification interface control signals, such as FRAME#, IRDY#, and TRDY#, are not part of the transaction itself, i.e., the information exchange, instead they control the physical PCI Local Bus. (PCI LBS, Appx. 65 at -686-687, -701, -947-949; Gafford Decl. at ¶¶ 16-31.)

5. ACQIS disputes EMC's SMF ¶15. Dr. Lindenstruth testified in the IPRs that a PCI bus transaction in the context of the claims requires only PCI address, data, command, and byte enables. (Ex. 5[2], Lindenstruth Dep. (8/28/15) at 339:18-25.) Dr. Lindenstruth testified that control signals, FRAME#, IRDY#, TRDY#, and DEVSEL# are not part of the transaction in his declaration to the PTAB (Dr. Lindentruth's annotations in original):

[2] All Exhibits cited herein are attached to the Declaration of James Brogan in Support of ACQIS's Opposition to EMC's Motion for Summary Judgment of Non-Infringement.

62. … A diagram of a PCI standard bus write transaction is set out in the portion of the PCI Local Bus standard below:

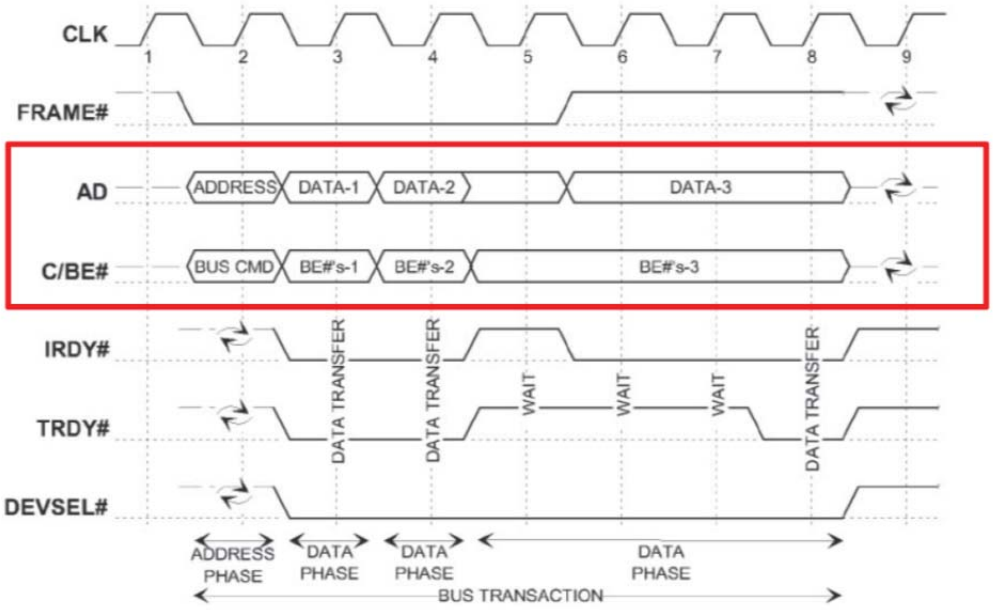

Figure 3-2: Basic Write Operation

(Lindenstruth '814 IPR Decl., D.I. 189-5 at ¶¶62, 114; Lindenstruth '873 IPR Decl., D.I. 189-4 at ¶¶64, 119.) Dr. Lindenstruth further testified in his IPR Declarations:

> I note that a PCI Bus is parallel and the claims discuss communicating PCI bus transactions serially, so the claims do not require that the PCI bus transaction occur on a PCI bus; they require the address and data phases of a PCI bus transaction, which include the PCI address and bus command information during the address phase and the PCI data and byte enables during the data phases.

(Lindenstruth '814 IPR Decl., D.I. 189-5 at ¶114 (citations omitted); Lindenstruth '873 IPR Decl., D.I. 189-4 at ¶119.)

6. ACQIS disputes EMC's SMF ¶16. In the IBM case, Mr. Gafford opined, "[w]hat the Chu disclosure defines as an encoded PCI transaction is not just the data in the transaction, but all the PCI signals necessary for the data to be transferred using the PCI bus. *See, e.g.*, '3,415, col. 15 ll. 57-62." (D.I. 505-20 at 83, 99, 167, 188.) Mr. Gafford's citation to the '3,415 patent confirms that, in addition to data, a PCI bus transaction requires a PCI address:

> *PCI address/data (AD) from the host PCI bus* is entered into FIFOs 1012 and 1017 before they are encoded by encoders 1022 and 1023. Encoders 1022 and 1023 format the *PCI address/data bits* to a form more suitable to parallel to serial conversion prior to transmittal on the XPBus.

(Ex. 6, '3,415 patent at col. 15:57-62 (emphasis added).)

7. ACQIS disputes EMC's SMF ¶17. Mr. Gafford testified that the PCI interface control signals FRAME#, IRDY#, and TRDY# are only necessary for data to be transferred over a physical PCI Local Bus and that interface control signals are not part of the transaction. Mr. Gafford testified, referencing FRAME#, IRDY#, and TRDY#:

> Again, these are part of managing the medium. They're not the transaction itself, but they certainly are the signals that, as with any -- as with other sorts of buses, are used to manage the medium so that information can be transferred.

(D.I. 505-20 at 80:18-23.)

8. ACQIS disputes EMC's SMF ¶19 to the extent EMC includes signals other than address, data, command, and byte enables as part of the transaction. (PCI LBS, Appx. 65 at -948; Gafford Report, Appx. 27 at ¶¶233-245; Gafford Decl. at ¶¶16-22.) The PCI Local Bus Specification describes interface control signals as control the physical PCI Local Bus and are not part of the transaction itself. (PCI LBS, Appx. 65 at -701, -711; Gafford Report, Appx. 27 at ¶245; Gafford Decl. at ¶¶21, 23-31.)

9. ACQIS disputes EMC's SMF ¶20 to the extent EMC includes signals other than address, data, command, and byte enables as part of the transaction. (PCI LBS, Appx. 65 at -948; Gafford Report, Appx. 27 at ¶¶233-245; Gafford Decl. at ¶¶16-22.) The PCI Local Bus Specification describes interface control signals as control the physical PCI Local Bus and are not part of the transaction itself. (PCI LBS, Appx. 65 at -701, -711; Gafford Report, Appx. 27 at ¶245; Gafford Decl. at ¶¶21, 23-31.)

10. ACQIS disputes EMC's SMF ¶21 to the extent EMC includes signals other than address, data, command, and byte enables as part of the transaction. (PCI LBS, Appx. 65 at -948; Gafford Report, Appx. 27 at ¶¶233-245; Gafford Decl. at ¶¶16-22.) The PCI Local Bus Specification describes interface control signals as control the physical PCI Local Bus and are not part of the transaction itself. (PCI LBS, Appx. 65 at -701, -711; Gafford Report, Appx. 27 at ¶245; Gafford Decl. at ¶¶21, 23-31.)

11. ACQIS disputes EMC's SMF ¶23 to the extent EMC includes a parity bit as part of the transaction. (PCI LBS, Appx. 65 at -948; Gafford Report at ¶¶215-223, 245; Gafford Decl. at ¶¶37-45.) For a transaction over a PCI Local Bus, the parity bit is sent after the address and data of the transaction and is used to detect errors in the communication of the transaction. Parity is only calculated on the address, data, command, and byte enable signals of the PCI Local Bus. (PCI LBS, Appx. 65 at -771, -686; Gafford Decl. at ¶¶21, 37-45.)

12. ACQIS disputes EMC's SMF ¶25 to the extent EMC includes a parity bit as part of the transaction. (PCI LBS, Appx. 65 at -948; Gafford Report at ¶¶215-223, 245; Gafford Decl. at ¶¶37-45.) For a transaction over a PCI Local Bus, the parity bit is sent after the address and data of the transaction and is used to detect errors in the communication of the transaction. Parity is only calculated on the address, data, command, and byte enable signals of the PCI Local Bus. (PCI LBS, Appx. 65 at -771, -686; Gafford Decl. at ¶¶21, 37-45.) Although parity generation is required by all PCI compliant devices, PCI compliant devices require a physical PCI Local Bus. (PCI LBS, Appx. 65 at -683, Ex. 9 at -795-860.)

13. ACQIS disputes EMC's SMF ¶27 to the extent EMC includes signals other than address, data, command, and byte enables as part of the transaction. (PCI LBS, Appx. 65 at -948; Gafford Report, Appx. 27 at ¶¶233-245; Gafford Decl. at ¶¶16-22.) The PCI Local Bus

Specification describes interface control signals as control the physical PCI Local Bus and are not part of the transaction itself. (PCI LBS, Appx. 65 at -701, -711; Gafford Report, Appx. 27 at ¶245; Gafford Decl. at ¶¶21, 23-31.)

14. ACQIS disputes EMC's SMF ¶28 to the extent EMC includes signals other than address, data, command, and byte enables as part of the transaction. (PCI LBS, Appx. 65 at -948; Gafford Report, Appx. 27 at ¶¶233-245; Gafford Decl. at ¶¶16-22.) The PCI Local Bus Specification describes interface control signals as control the physical PCI Local Bus and are not part of the transaction itself. (PCI LBS, Appx. 65 at -701, -711; Gafford Report, Appx. 27 at ¶245; Gafford Decl. at ¶¶21, 23-31.)

15. ACQIS disputes EMC's SMF ¶29. Mr. Gafford opined that [redacted] (Gafford Report, Appx. 27 at ¶248; *see also id.* at ¶¶246-270.) These encoded bits are communicated in parallel form prior to transmission over the PCI Express channels. (Gafford Report, Appx. 27 at ¶¶224-232; Gafford Decl. at ¶¶52-65.) Mr. Gafford's opinions are supported by the PCI Express Specifications, the PCI Express Technology treatise, and the PCI Special Interest Group PCI Express Architecture Overview Presentation. (*Id.*) In his report, Mr. Gafford summarized his opinions as to how PCI Express communicates PCI Local Bus Specification interface control signals in the chart reproduced below:

(Gafford Report, Appx. 27 at ¶270.)

16. ACQIS disputes EMC's SMF ¶30. As explained above in ¶15, Mr. Gafford opined that [redacted] (Gafford Report, Appx. 27 at ¶248; *see also id.* at ¶¶246-270.)

17. ACQIS disputes EMC's SMF ¶31. As explained in ¶15 above, Mr. Gafford opined that the [redacted] (Gafford Report, Appx. 27 at ¶¶246-270.)

18. ACQIS disputes EMC's SMF ¶32. As explained in ¶15 above, Mr. Gafford opined that the [redacted] (Gafford Report, Appx. 27 at ¶¶246-270.)

19. ACQIS disputes EMC's SMF ¶33. As explained in ¶15 above, Mr. Gafford opined that the [redacted] (Gafford Report, Appx. 27 at ¶¶246-270.)

20. ACQIS disputes EMC's SMF ¶35. In the PCI Local Bus Specification, address precedes data in a transaction. In a PCI Express transaction the address always precedes data. (Gafford Dep. (5/18/18), Ex. 1 at 546:11-19 [redacted]); *see also id.* at 545:25-549:22; Gafford Report Appx. 27 at ¶¶235-237 (showing the address of the address of the packet header preceding the data). As shown in the PCI Express Spec., the address contained in the transaction layer packet header always precedes that data of the transaction. (PCI Express Spec., Appx. 56 at -6273, -6289-6291.)

21. ACQIS disputes EMC's SMF ¶39. Evidence in the record shows that PCI Express "conveys bits that represent parity." (Gafford Dep. (5/18/18), Ex. 1 at 488:13-16.) The Cyclic Redundancy Check used in PCI Express is in accordance with the PCI Local Bus Specification: [redacted] (Gafford Dep. (5/18/18), Ex. 1 at 498:4-9; *see also id.* at 488:13-498:9; PCI Express Spec., Ex. 3 at -6370-6376.)

22. ACQIS disputes EMC's SMF ¶40. PCI Express communicates command bits indicating the type of PCI bus transaction to be executed in accordance with the PCI Local Bus Specification. (Gafford Report, Appx. 27 at ¶¶238-242; Gafford Decl. at ¶47.)

23. ACQIS disputes EMC's SMF ¶47. ACQIS contends that a PCI bus transaction in accordance with the PCI Local Bus Specification requires an address and data transfer along with command and byte enable information to identify the type of transaction and the valid bytes of data. (Gafford Decl. at ¶¶16-22.)

24. ACQIS disputes EMC's SMF ¶49 to the extent EMC interprets the Court's construction to require a complete PCI bus transaction be converted into serial form at once. (D.I. 389 at 10-16.)

25. ACQIS disputes EMC's SMF ¶50 because it is incomplete. Although PCI Express is a "fully serial interface," prior to transmission over the serial interface, PCI Express serializes from a parallel form all data communicated over the serial interface. (Hospodor Dep., Ex. 2 at 184:25-186:3, 202:23-203:5; Hospodor Report, Appx. 33 at ¶262; Bhatt Report Appx. 35 at ¶105, Bhatt Dep., Ex. 7 at 160:23-161:12; PCI Express Spec. Appx. 56 at -6390-6392, -6266 ("The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion.").)

26. ACQIS disputes EMC's SMF ¶52. Mr. Gafford testified that [redacted] (D.I. 505-9 at 527:10-21.) Mr. Gafford's Report and Declaration also illustrate how parallel PCI bus transactions are serialized from a parallel form. (Gafford Report, Appx 27 at ¶¶224-232; Gafford Decl. at ¶¶52-66.)

27. ACQIS disputes EMC's SMF ¶53. Mr. Gafford's report states, [redacted]

[redacted] (Gafford Report, Appx. 27 at ¶229 (emphasis added); *see also id.* at ¶¶224-232.) Mr. Gafford's Declaration further establishes that PCI bus transactions are communicated in parallel form in the accused products prior to parallel-to-serial conversion. (Gafford Decl. at ¶¶52-72.) The PCI Express Specification also shows that PCI bus transactions are communicated in parallel form prior to parallel-to-serial conversion:

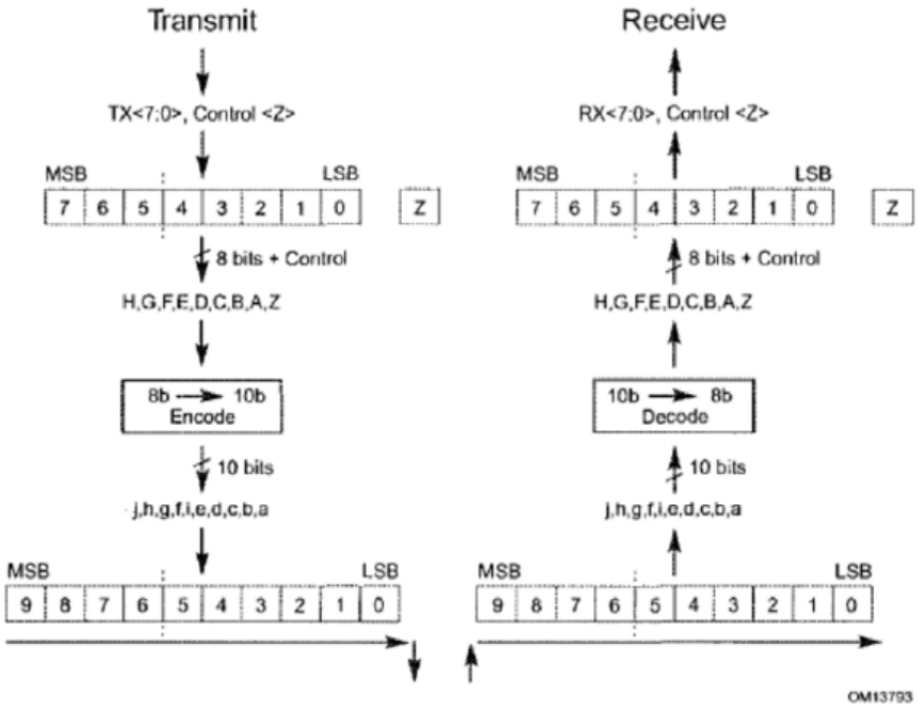

Figure 4-2: Character to Symbol Mapping

(PCI Express Spec., Appx. 56 at -6392; Gafford Report, Appx. 27 at ¶227-28.)

28. ACQIS disputes EMC's SMF ¶54. EMC does not point to any intrinsic support to show that "in the context of the asserted patents, the term 'parallel' refers to how something is communicated, not how it is stored." Furthermore, Mr. Gafford's Declaration shows that data is

stored in registers in PCI Express and data is moved from those registers in parallel form. (Gafford Decl. at ¶¶60-65; Gafford Report at ¶¶224, 414; Ex. 9 at 646:14-647:2.)

29. ACQIS disputes EMC's SMF ¶56. A PCI bus transaction in accordance with the PCI Local Bus Specification must have at least 32 bits of address *and* data along with command and byte enable information. (PCI LBS, Appx. 65 at -685-686, -711, -948.)

30. ACQIS disputes EMC's SMF ¶58. In PCI Express, converting encoded 10-bit symbols from a parallel form is parallel-to-serial conversion. (Gafford Report, Appx 27 at ¶¶224-232; Gafford Decl. at ¶¶52-66; PCI Express Spec. Appx. 56 at -6390-6392, -6266.)

31. ACQIS disputes EMC's SMF ¶65. The asserted patents describe command and byte enables as control bits. (Gafford Dep. (5/3/18), Ex. 4 at 94:23-95:6; Gafford Decl. at ¶¶73-81; Gafford Report ¶239; '330 Patent, Appx. 15 at FIGs. 36-37, col. 19:26-20:8; '873 patent, Appx. 9 at FIG. 10, col. 17:4-60, 20:44-47.)

32. ACQIS disputes EMC's SMF ¶68. Mr. Gafford opined that [redacted] (Gafford Report, Appx. 27 at ¶248; *see also id.* at ¶¶246-270.) These encoded bits are communicated in parallel form prior to transmission over the PCI Express channels. (Gafford Report, Appx. 27 at ¶¶224-232; Gafford Decl. at ¶¶52-65.) Mr. Gafford's opinions are supported by the PCI Express Specifications, the PCI Express Technology treatise, and the PCI Special Interest Group PCI Express Architecture Overview Presentation. (*Id.*) In his report, Mr. Gafford summarized his opinions as to how PCI Express communicates PCI Local Bus Specification interface control signals in the chart reproduced below:

(Gafford Report, Appx. 27 at ¶270.)

33. ACQIS disputes EMC's SMF ¶69. As explained above in ¶31, Mr. Gafford opined that [redacted] (Gafford Report, Appx. 27 at ¶248; *see also id.* at ¶¶246-270.)

34. ACQIS disputes EMC's SMF ¶70. As explained above in ¶31, Mr. Gafford opined that [redacted] (Gafford Report, Appx. 27 at ¶248; *see also id.* at ¶¶246-270.)

Dated: August 21, 2018

Respectfully submitted,

/s/James P. Brogan
James P. Brogan

CERTIFICATE OF SERVICE

I hereby certify that this document filed through the CM/ECF system will be sent electronically to the registered participants as identified on the Notice of Electronic Filing (NEF) and paper copies will be sent to those indicated as non-registered participants on August 21, 2018.

/s/ *James P. Brogan*
James P. Brogan